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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,922	YEH, TA-CHIA	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined.

Drawings

2. The drawings are objected to because of insufficient margins. See 37 C.F.R. § 1.84(g). Also, in Figs. 2 and 3 TEST_MOD should be changed to TEST_MODE.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

a. Page numbers missing throughout disclosure (i.e. Abstract, Specification, Claims, and Drawings). Page numbers should be added.

b. There should be an extra double space at the beginning of each paragraph.

c. Paragraph 17, CLK" should be changed to CLK'.

d. Paragraph 20, In reference to Fig. 3, the first delay chain 314 is not installed in front of multiplexer 316 as the specification states. It is installed in front of multiplexer 318. Correction is required.

e. Paragraph 20, in the phrase "groups do not operate synchronous", change synchronous to synchronously.

f. Paragraph 22, the statement, "The embodiments of the present invention disclose the method to input the scanning test signals into each flip-flop group asynchronously in a predetermined sequence". The Examiner does not know if this are test data signals or test clock signals. Clarification and correction is required in response to this office action.

Appropriate correction is required.

Claim Objections

4. The claims are objected to because of improper indentation. Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation, 37 CFR 1.75(i). Also, see MPEP 608.01(i)-(p).

5. Claim 14 is objected to because of the following informalities: "when logic operation" should recite "when a logic operation". Appropriate correction is required.

6. Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of independent claim 16. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The limitation of claim 17 is basically the same as the "operating the second flip-flop group according to a delayed first scanning test clock signal" limitation of claim 16.

Claim Rejections - 35 USC § 112

The following is a quotation of the **first paragraph** of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 1-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1:

The limitation "in a predetermined sequence" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner does understand what is meant by "in a predetermined sequence" and the specification does not shed any light on this. The only reference to this limitation is in paragraph 22 and this does not disclose how this is done. Clarification and correction is required in response to this office action.

Claim 2:

The claim limitation "during the scanning test, the scanning test clock signal is asynchronously input into the first flip-flop group and the second flip-flop group in sequence to be their clock signal" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention because nowhere in the specification is the test clock signal asynchronously inputted into the first flip-flop group. Clarification and correction is required in response to this office action.

Claim 4:

The claim limitation "first multiplexer coupled with the first delay device and the first flip-flop group, for selectively outputting the first clock signal or the delayed scanning test clock signal to the first flip-flop group" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention because nowhere in the

specification is the first delay device and the first flip-flop group coupled as to selectively output the first clock signal or the delayed scanning test clock signal to the first flip-flop group. Because of the lack of enablement issues these claims will not be further examined on the merits. Clarification and correction is required in response to this office action.

Claim 5:

The claim limitation "the first flip-flop group and the second flip-flop group are serially connected in a scan chain" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention because nowhere in the specification is "the first flip-flop group and the second flip-flop group are serially connected in a scan chain". Clarification and correction is required in response to this office action.

Claims 8-10:

These claims recite limitations that are not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention because nowhere in the specification is "a functional input signal" or a scan input signal" disclosed. The specification also does not disclose "a first unit". Because of the lack of enablement issues these claims will not be further examined on the merits. Clarification and correction is required in response to this office action.

Claim 12:

a.) The limitation "in a predetermined sequence" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner does understand what is meant by "in a predetermined sequence" and the specification does not shed any light on this. The only reference to this limitation is in paragraph 22 and this does not disclose how this is done. Clarification and correction is required in response to this office action.

b.) The limitation "through the first delay device and the second delay device, a scanning test clock signal is asynchronously input into the first flip-flop group" is not enabled by the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Nowhere in the disclosure does any delay device input any signal to the first flip-flop group. Clarification and correction is required in response to this office action.

Claims 3, 6, 7, 11-15:

These claims are also rejected because they depend on rejected claims and have the same problems of lack of enablement.

The following is a quotation of the **second paragraph** of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

a.) The limitation "in a predetermined sequence" renders the claim indefinite. The Examiner does understand what is meant by "in a predetermined sequence" and the specification does not shed any light on this. The only reference to this limitation is in paragraph 22 and this does not disclose how this is done. Clarification and correction is required in response to this office action.

b.) The limitation "wherein during a scanning test, a scanning test clock signal is asynchronously input into the clock domains in a predetermined sequence" renders the claim indefinite. From the claim language the Examiner does not know how this is functionally achieved. For reason of examination the Examiner assumes this means the scanning test clock signal is delayed into the clock domains.

c.) The limitation "wherein during a scanning test, a scanning test clock signal is asynchronously input into the clock domains in a predetermined sequence" is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the elements that make the limitation functionally possible.

d.) This claim recites the limitation "the clock domains" in line 6. There is insufficient antecedent basis for this limitation in the claim. This should be "the plurality of clock domains".

Claim 2:

a.) The claim limitation "in sequence to be their clock signal" renders the claim indefinite. The Examiner doesn't know what this means.

b.) This claim recites the limitation "the logic operation" in line 8. There is insufficient antecedent basis for this limitation in the claim.

c.) This claim recites the limitation "the second clock signal" in lines 10-11. There is insufficient antecedent basis for this limitation in the claim.

d.) The limitation "during the scanning test, the scanning test clock signal is asynchronously input into the first flip-flop group and the second flip-flop group in sequence to be their clock signal" is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the elements that make the limitation functionally possible.

Claim 5:

The claim limitation "the first flip-flop group and the second flip-flop group are serially connected in a scan chain" renders the claim indefinite because the Examiner interpret whether the first flip-flop group and the second flip-flop group **each** are serially connected in a scan chain or if first flip-flop group is serially connected to the second flip-flop group to form a scan chain. Clarification and correction is required in response to this office action.

Claim 6:

a.) The claim limitation "in sequence to be their clock signal" renders the claim indefinite. The Examiner doesn't know what this means.

b.) The limitation "during the scanning test, the scanning test clock signal is asynchronously input into the first flip-flop group and the second flip-flop group in sequence to be their clock signal." is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the elements that make the limitation functionally possible.

c.) This claim recites the limitation "the first flip-flop group and the second flip-flop group ". There is insufficient antecedent basis for this limitation in the claim. This should read "the at least one first flip-flop group of the first clock domain" and "the at least one first flip-flop group of the second clock domain", respectively.

Claim 12:

a.) The claim limitations "a first delay device for outputting a first delayed scanning test clock signal" and "a second delay device for outputting a second delayed scanning test clock signal" renders the claim indefinite because the inputs are not defined. For purpose of examination the Examiner is assuming, using Fig. 3 as a guide, that the input is TEST_CLK1. Correction is required in response to this office action.

b.) The claim limitation "wherein during a scanning test, through the first delay device and the second delay device, a scanning test clock signal is asynchronously

input into the first flip-flop group, the second flip-flop group and the third flip-flop group in a predetermined sequence is extremely confusing and, therefore, renders the claim vague and indefinite. Firstly, the limitation "through the first delay device and the second delay device, a scanning test clock signal is asynchronously input..." is confusing because in the previous limitations the "a first delay device outputs a first delayed scanning test clock signal" and "a second delay device outputs a second delayed scanning test clock signal". Now this limitation states there's a different clock (i.e. a scanning test clock signal, not previously defined) supplied to the flip-flop groups. Which one is it? Secondly, a major deficiency in this limitation is that it does not define which of the **different** outputs of the first and second delay devices (i.e. a first delayed scanning test clock signal and a second delayed scanning test clock signal, respectively) and are inputted to which flip-flop group. Thirdly, "in a predetermined sequence is indefinite because it is not clear what that means. The specification also does not elaborate on this. Lastly, nowhere in the disclosure does any delay device input any signal to the first flip-flop group (also, the subject of the 112/1st paragraph rejection above).

c.) The limitation "a scanning test clock signal is asynchronously input into the first flip-flop group..." is incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the elements that make the limitation functionally possible. The flip-flop groups receives "a first clock signal" and "a second clock signal", now somehow during scanning test the flip flop groups receive a new scanning test clock signal that is

asynchronously input to the groups. How is that achieved? That's what's missing. Hint: adding the multiplexers and test mode signal to the claim and connecting them according to Fig. 3 would help.

For the purpose of examination the Examiner is using Fig. 3 to aid in the interpretation of the claims.

Claim 15:

This limitation "the scanning test clock signal is the first clock signal or the second clock signal is vague and indefinite. Throughout the specification the first clock signal and the second clock signal has been referred to as CLK1 and CLK2 of Figs. 2 and 3. The scanning test clock signal in Fig. 2 is the delayed CLK1 CLK'. The scanning test clock signal in Fig. 3 is TEST_CLK1.

Claims 3, 4, 7-11, 13, 14:

These claims are also rejected because they depend on rejected claims and have the same problems of indefiniteness.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-3, 5-7, 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art, hereinafter AAPA, in view of Lurkins (US006964002), hereinafter Lurkins.

Claims 4, 8-10 Note:

These claims will not be further examined on the merits as per the 35 U.S.C. 112/1st paragraph rejections present above.

Claims 1 and 16:

AAPA teaches a plurality of clock domains (Fig. 1, 110 and 150) corresponding respectively to a plurality of clock signals (Fig. 1, CLK1, CLK2) and comprising at least one flip-flop group per each clock domain (Fig. 1, 118 for 110, 158 for 150). wherein during a scanning test, a scanning test clock signal is asynchronously input into the clock domains in a predetermined sequence. AAPA does not explicitly teach "during a scanning test, a scanning test clock signal is asynchronously input (i.e. delayed input as per 112/2nd rejection point b.) into the clock domains in a predetermined sequence". However, AAPA does teach "during a scanning test, a *non-delayed* scanning test clock signal is input into the clock domains". Lurkins teaches in an analogous art a base clock signal enters the MUX 20 on connection 15 and is split into two branches 90 (Fig.

1, LOG1) and 92 (Fig. 1, TEST_CLK). Branch 90 (Fig. 1, LOG1) goes directly into a switch 98 (Fig. 1, MUX 116) while branch 92 (Fig. 1, TEST_CLK) enters a delaying unit 94. The delaying unit 94 can be a delay cell, an inverter, or other mechanism that retains the shape and frequency of the clock signal. Lurkins also teaches the delayed signal from the delaying unit 94 enters switch 98 (Fig. 1, MUX 116) via connection 96 (delayed test clock signal). Lurkins further teaches a selection line 100 (Fig. 1, TEST_MODE) allows a user to set switch 98 so that either the undelayed clock signal from connection 90 (Fig. 1, LOG1) or the delayed clock signal from connection 96 (delayed test clock signal) is placed on output 30. (Col. 5, ll. 45-58, Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify AAPA to add Lurkins' delaying unit 94 in order to delay the AAPA's TEST_CLK connection to the multiplexers 116, 154 and 156 of Fig. 1. The artisan would be motivated to do so because introducing Lurkins' delaying unit 94 to the AAPA's TEST_CLK will enable AAPA to reduce the chances of race conditions occurring between the different flip-flop groups (scan chains) during scan testing mode. The artisan would also be motivated to do so because it would enable AAPA to switch between a functional clock (LOG1) and a delayed test clock (delayed TEST_CLK outputted from Lurkins' delaying unit 94) during scan testing mode. (See Lurkins Col. 1, ll. 17-19, l. 51 to col. 2, ll. 54, col. 3, ll. 11-23).

Claim 2:

AAPA teaches a first flip-flop group (Fig. 1, 118) that receives the first clock signal (Fig. 1, CLK1), a second flip-flop group (Fig. 1, 120) and a first logic gate group

(Fig. 1, 112) coupled with the first clock signal (Fig. 1, CLK1) for generating a first logic signal (Fig. 1, LOG1), wherein during *the logic operation* (not defined), the first flip-flop group (Fig. 1, 118) receives the first clock signal (Fig. 1, CLK1) as its clock signal, the second flip-flop group (Fig. 1, 120) receives *the second clock signal* (not defined, assumed to be LOG1) as its clock signal. AAPA in view of Lurkins teaches during the scanning test, the scanning test clock signal is asynchronously input (i.e. delayed input as per claim 1 112/2nd rejection point b.) into the first flip-flop group and the second flip-flop group in sequence to be their clock signal.

Claim 3:

AAPA in view of Lurkins teaches a first delay device (Lurkins' delaying unit 94) coupled with the scanning test clock signal (Fig. 1, TEST_CLK) for delaying the scanning test clock signal and a first multiplexer (Fig. 1, MUX 116) coupled with the first logic gate group (Fig. 1, 112), the first delay device (Lurkins' delaying unit 94), and the second flip-flop group (Fig. 1, 120), for selectively outputting the first logic signal or the delayed scanning test clock signal to the second flip-flop group.

Claim 5:

AAPA teaches the first flip-flop group and the second flip-flop group are serially connected in a scan chain. (¶ 6).

Claim 6:

AAPA in view of Lurkins teaches a first clock domain (Fig. 1, 110) coupled with a first clock signal (Fig. 1, CLK1) comprising at least one first flip-flop group (Fig. 1, 118) and a second clock domain (Fig. 1, 150) coupled with a second clock signal (Fig. 1,

CLK2) comprising at least one second flip-flop group (Fig. 1, 158), wherein during the scanning test, the scanning test clock signal is asynchronously input (i.e. delayed input as per claim 1 112/2nd rejection point b.) into the first flip-flop group and the second flip-flop group in sequence to be their clock signal.

Claim 7:

AAPA in view of Lurkins a first delay device (Lurkins' delaying unit 94) coupled with the scanning test clock signal (Fig. 1, TEST_CLK) for delaying the scanning test clock signal and a first multiplexer (Fig. 1, MUX 116) coupled with the first delay device (Lurkins' delaying unit 94) and the second flip-flop group (Fig. 1, 120), for selectively outputting the second clock signal or the delayed scanning test clock signal to the second flip-flop group.

Claim 11:

AAPA teaches scanning test clock signal is one of the clock signals. (Fig. 1).

Claim 12:

AAPA teaches **a first clock domain** (Fig. 1, 110) that receives **a first clock signal** (Fig. 1, CLK1) comprising: **a first flip-flop group** (Fig. 1, first flip-flop group 118) that receives **the first clock signal** (Fig. 1, CLK1) and **a second flip-flop group** (Fig. 1, second flip-flop group 120). AAPA also teaches **a second clock domain** (Fig. 1, 150) that receives **a second clock signal** (Fig. 1, CLK2) comprising: **a third flip-flop group** (Fig. 1, a third flip-flop group 158) that receives **the second clock signal** (Fig. 1, CLK2).

AAPA does not explicitly teach "**a first delay device** for outputting a first delayed scanning test clock signal, **a second delay device** for outputting a second delayed scanning test clock signal, and during a scanning test, through the first delay device and the second delay device, a scanning test clock signal is asynchronously input (i.e. delayed input as per claim 1, 112/2nd rejection, point b.) into, the second flip-flop group and the third flip-flop group in a predetermined sequence". However, AAPA does teach "during a scanning test, a *non-delayed* scanning test clock signal is input into the second flip-flop group and the third flip-flop group". Lurkins teaches in an analogous art a base clock signal enters the MUX 20 on connection 15 and is split into two branches 90 (Fig. 1, LOG1, CLK2) and 92 (Fig. 1, TEST_CLK). Branch 90 (Fig. 1, LOG1) goes directly into a switch 98 (Fig. 1, MUXes 116, 154) while branch 92 (Fig. 1, TEST_CLK) enters a delaying unit 94. The delaying unit 94 can be a delay cell, an inverter, or other mechanism that retains the shape and frequency of the clock signal. Lurkins also teaches the delayed signal from the delaying unit 94 enters switch 98 (Fig. 1, MUX 116) via connection 96 (delayed test clock signal). Lurkins further teaches a selection line 100 (Fig. 1, TEST_MODE) allows a user to set switch 98 so that either the undelayed clock signal from connection 90 (Fig. 1, LOG1) or the delayed clock signal from connection 96 (delayed test clock signal) is placed on output 30. (Col. 5, ll. 45-58, Fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify AAPA to add Lurkins' delaying unit 94 in order to delay the AAPA's TEST_CLK connection to the multiplexers 116, 154 and 156 of Fig. 1. The artisan would be motivated to do so because introducing Lurkins' delaying unit 94 to the AAPA's

TEST_CLK will enable AAPA to reduce the chances of race conditions occurring between the different flip-flop groups (scan chains) during scan testing mode. The artisan would also be motivated to do so because it would enable AAPA to switch between a functional clock (LOG1) and a delayed test clock (delayed TEST_CLK outputted from Lurkins' delaying unit 94) during scan testing mode. (See Lurkins Col. 1, ll. 17-19, l. 51 to col. 2, ll. 54, col. 3, ll. 11-23).

Claim 13:

AAPA in view of Lurkins teaches the first delayed scanning test clock signal is prior to or following the second delayed scanning test clock signal in that the amount of delay in each of Lurkins' delaying units 94 is a design choice based on the needs of the design.

Claim 14:

AAPA teaches a first logic gate group coupled with the second flip-flop group, for outputting a first logic signal according to the first clock signal; and the second flip-flop group operates according to the first logic signal when *a* logic operation is executed.

Claim 15:

AAPA teaches the scanning test clock signal is the first clock signal or the second clock signal. (Fig. 1).

Claim 17:

This claim is rejected as per the rejection of claims 1 and 16 above, since it does not further limit claim 16.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Huth et al. (US-6901544) and Kasahura (US-2002/0029361) teaches using delay elements to delay a clock to a second scan chain for resolving skew and/or race condition problems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 3/24/06
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100